

High speed readout for spin-filtering experiments

ANKE/PAX Workshop on Spin Physics

29 May - 1 June 2007

IUSS, Via Scienze 41b Ferrara, Italy

Luca Barion

INFN Ferrara/IKP Julich

VME system

- 5 MHz ADC clock
- 0,5 ms deadtime
- expensive
- No common-mode

LVDS System

Test system (Test pulse/Alpha particles)

- 1 Si strip detector
- 2 Front-end cards (developed by S.Merzliakov)
- 2 Repeater cards (developed by S.Merzliakov)
- 1 Vertex board (developed/produced by ZEL⁽¹⁾)
- 1 LVDS crate (developed/produced by ZEL⁽¹⁾)

⁽¹⁾ Zentralinstitut für Elektronik - Forschungszentrum Jülich

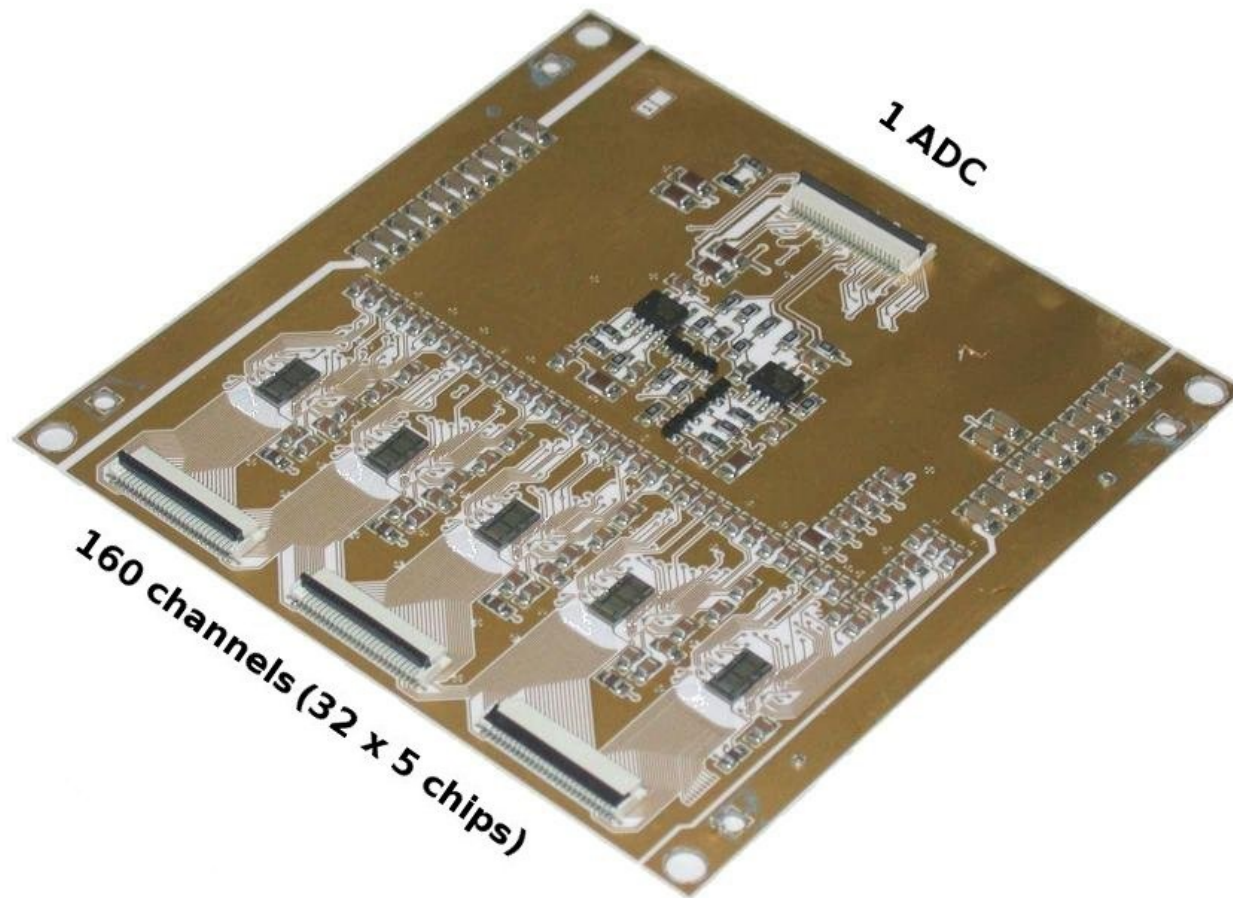
Test system (Test pulse/Alpha particles)

- **1 Detector** (one 300 μm layer)
- 2 Front-end cards
- 2 Repeater cards
- 1 Vertex board (2 sequencers + 2 ADC)
- 1 LVDS crate (+controller, diskless pc, acquisition pc)



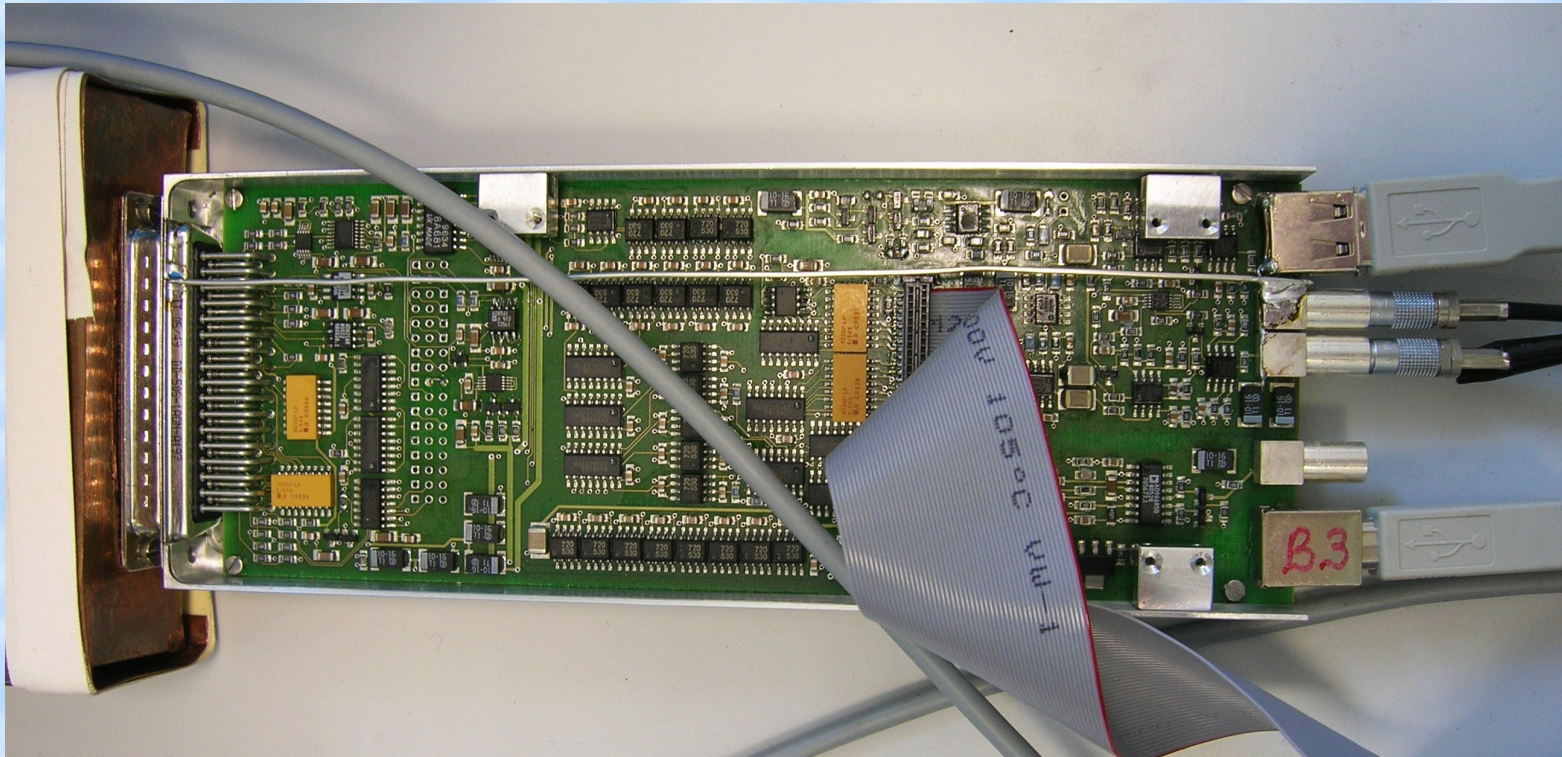
Test system (Test pulse/Alpha particles)

- 1 Detector (one 300 μm layer)
- 2 **Front-end cards**
- 2 Repeater cards
- 1 Vertex board (2 sequencers + 2 ADC)
- 1 LVDS crate (+controller, diskless pc, acquisition pc)



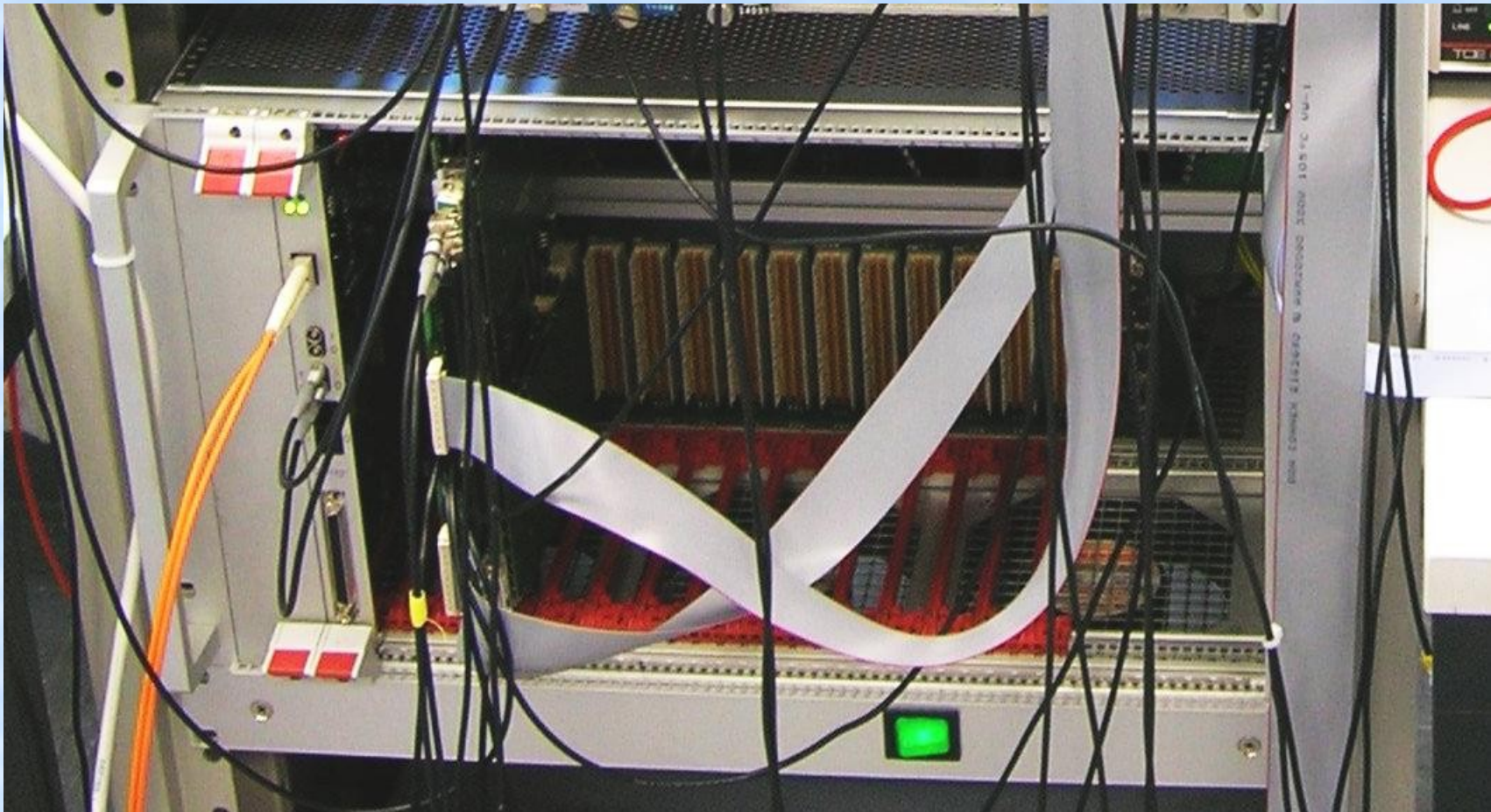
Test system (Test pulse/Alpha particles)

- 1 Detector (one 300 μm layer)
- 2 Front-end cards
- 2 **Repeater cards**
- 1 Vertex board (2 sequencers + 2 ADC)
- 1 LVDS crate (+controller, diskless pc, acquisition pc)

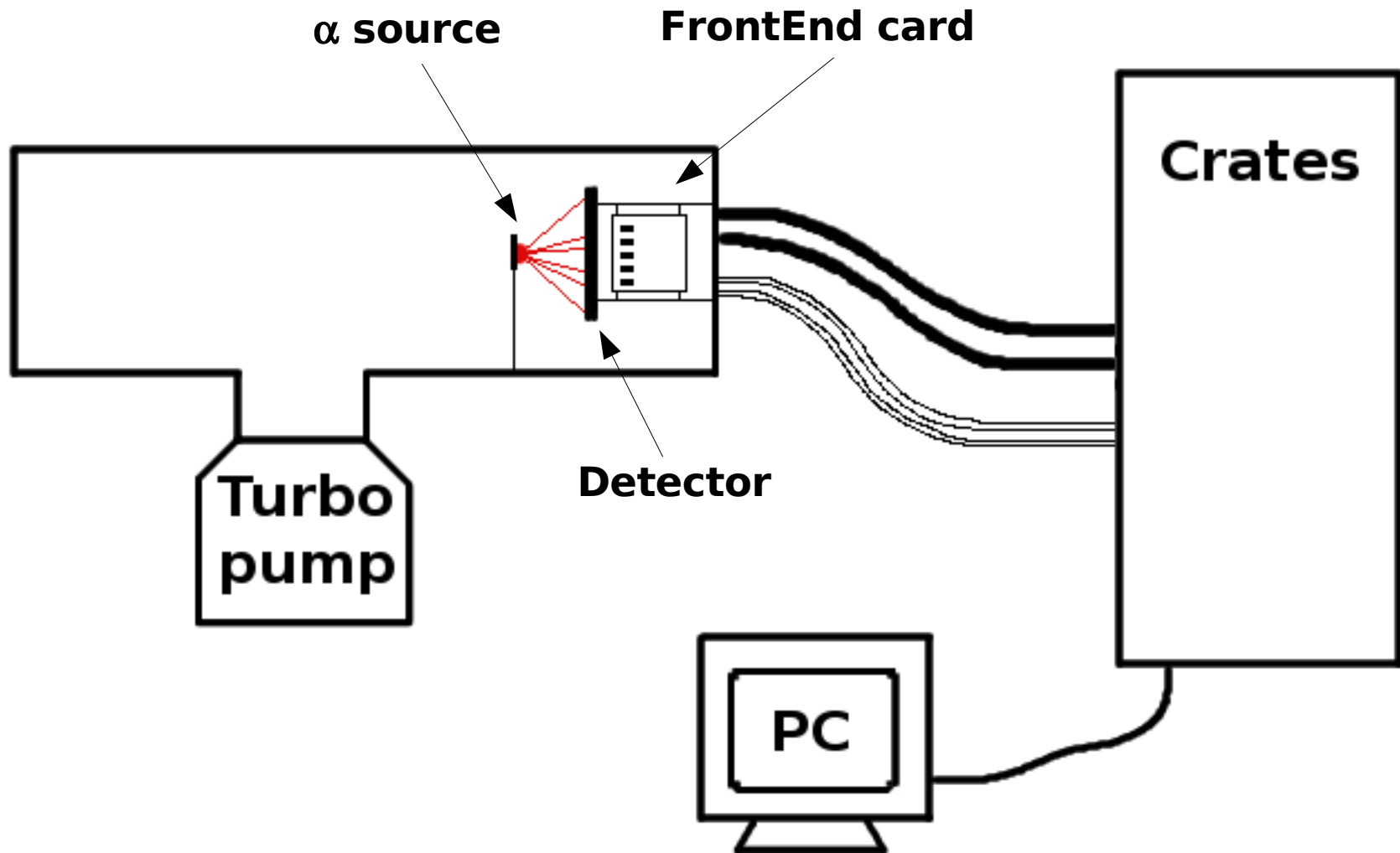


Test system (Test pulse/Alpha particles)

- 1 Detector (one 300 μm layer)
- 2 Front-end cards
- 2 Repeater cards
- **1 Vertex board** (1 sequencer + 2 ADC)
- **1 LVDS crate** (**controller**, diskless pc, acquisition pc)

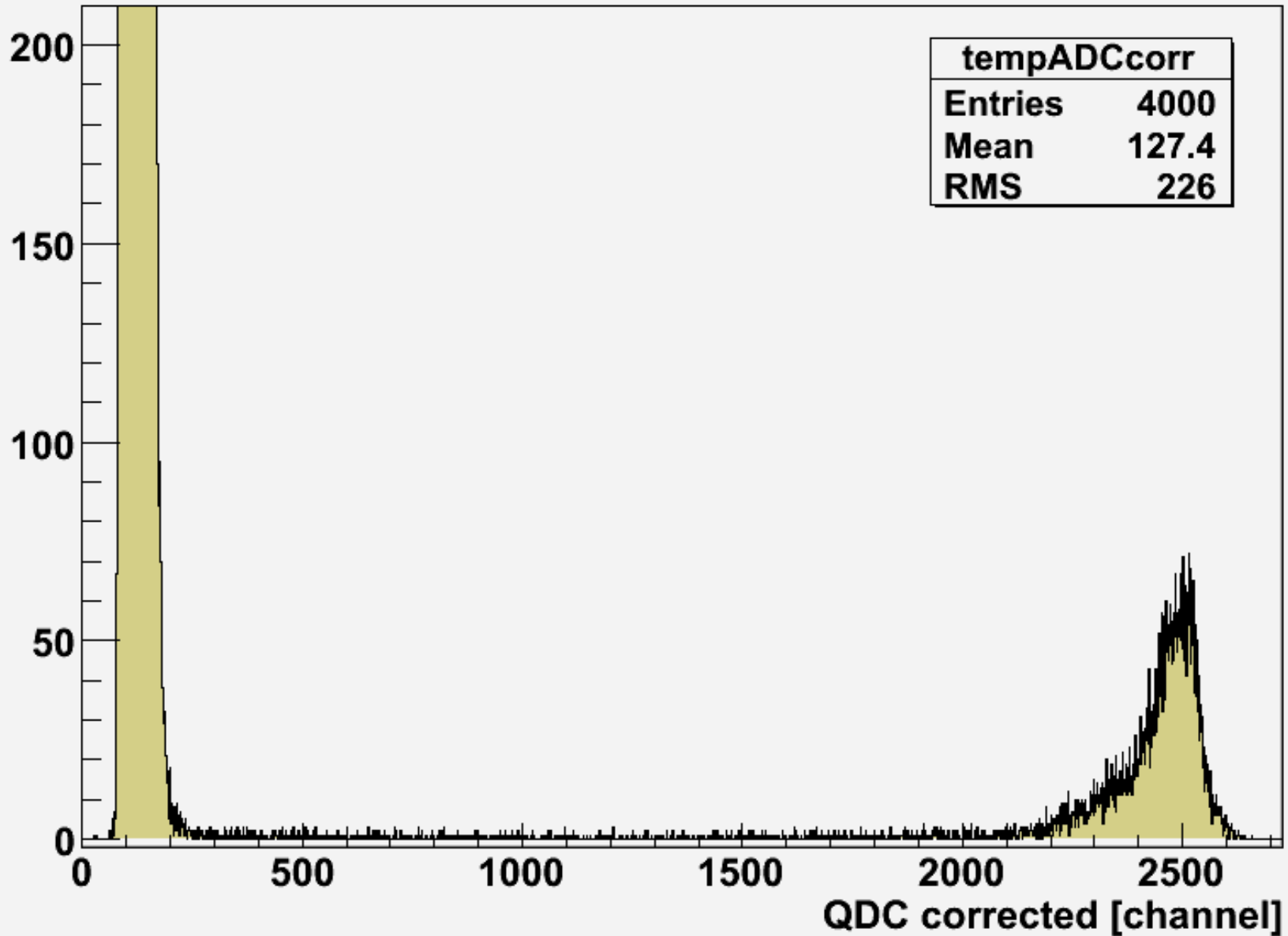


Test system setup



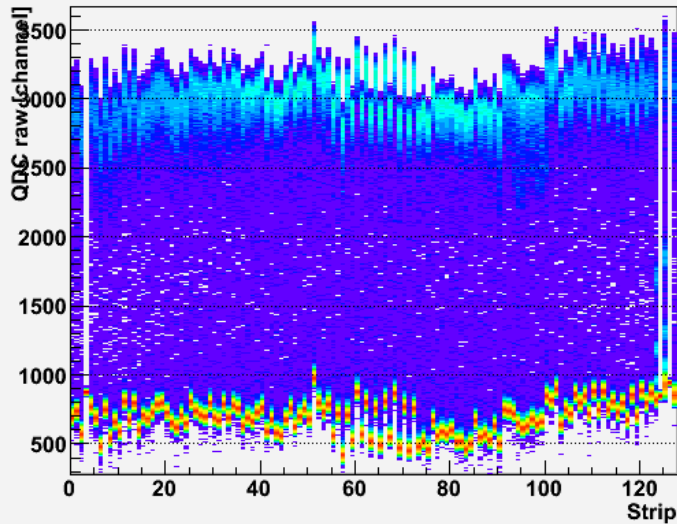
Single strip spectrum

segment corrected L1_L_Pos 050 (ADC=SpADC_1 input=0 channel=050)

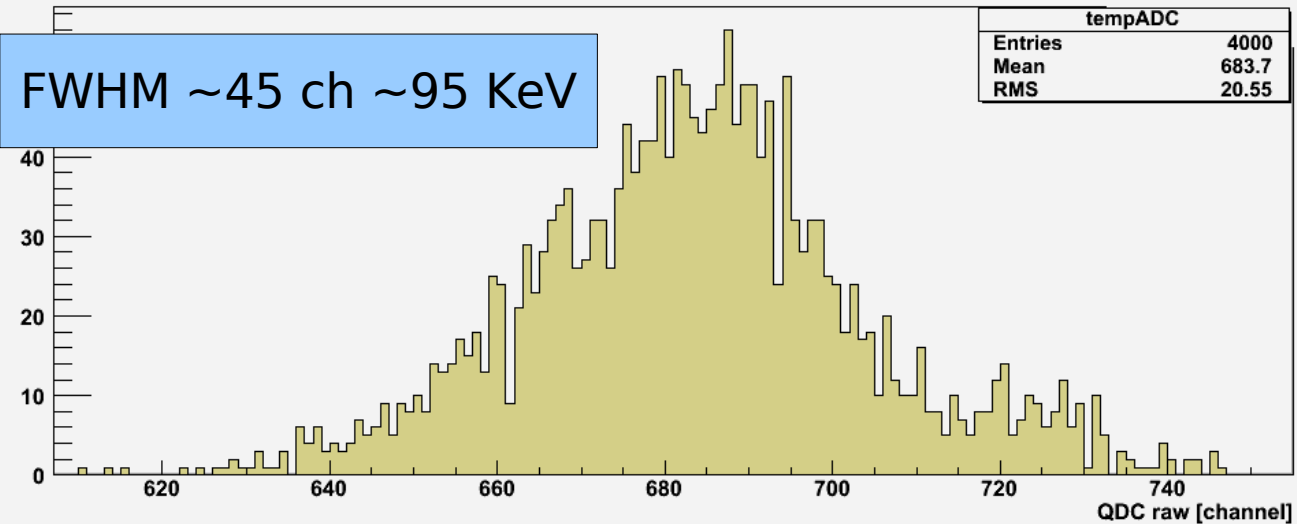


Pedestals, 2 Mhz ADC clock

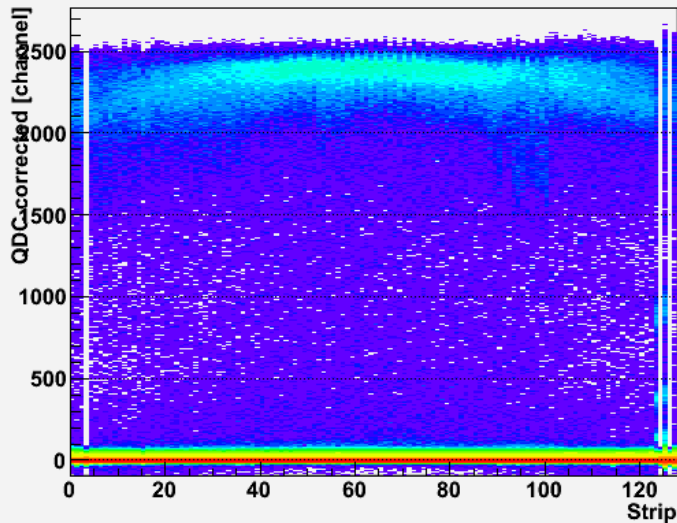
Side L1_L_Pos Profile (ADC=SpADC_1)



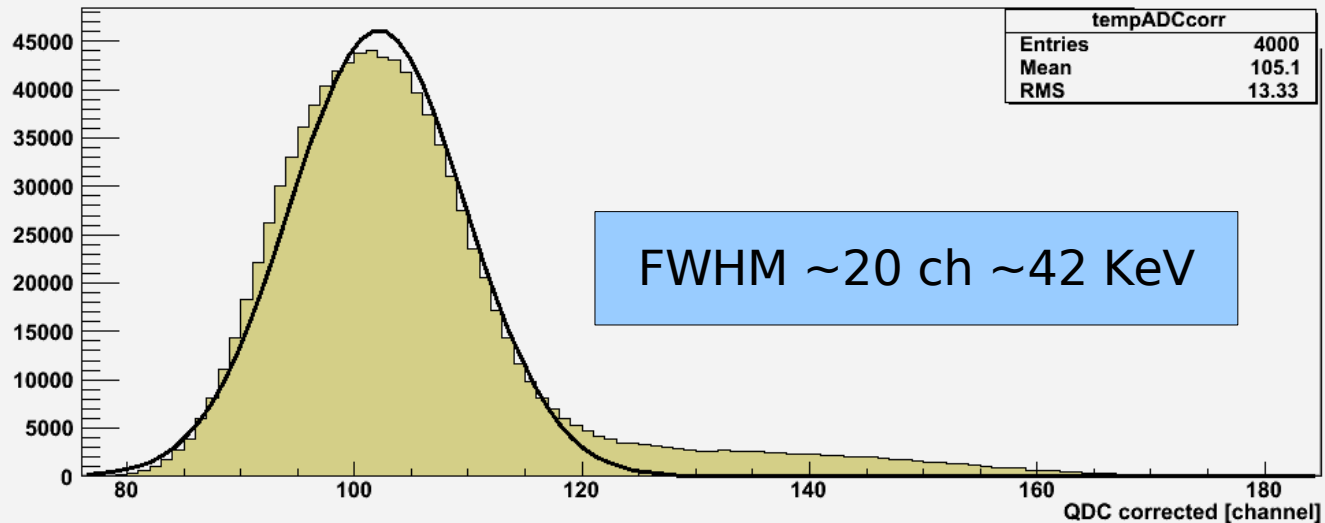
Segment QDC L1_L_Pos 050 (ADC=SpADC_1 input=0 channel=050)



Side L1_L_Pos Corrected Profile (ADC=SpADC_1)

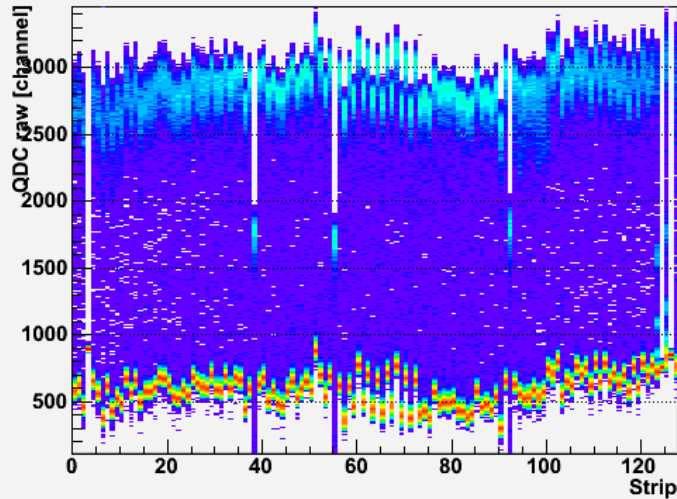


segment corrected L1_L_Pos 050 (ADC=SpADC_1 input=0 channel=050)

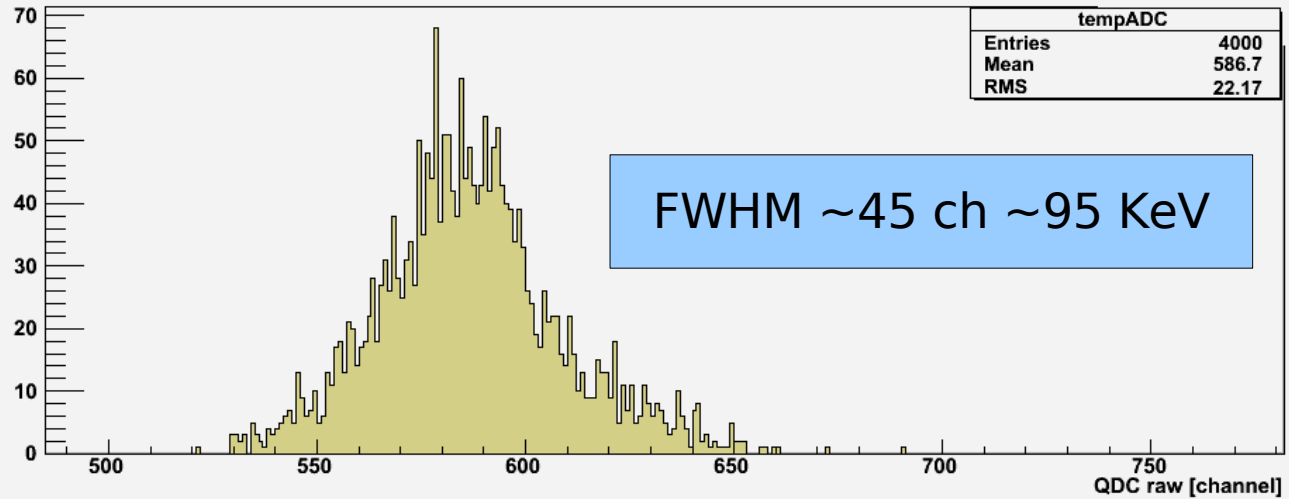


Pedestals, 10 Mhz ADC clock

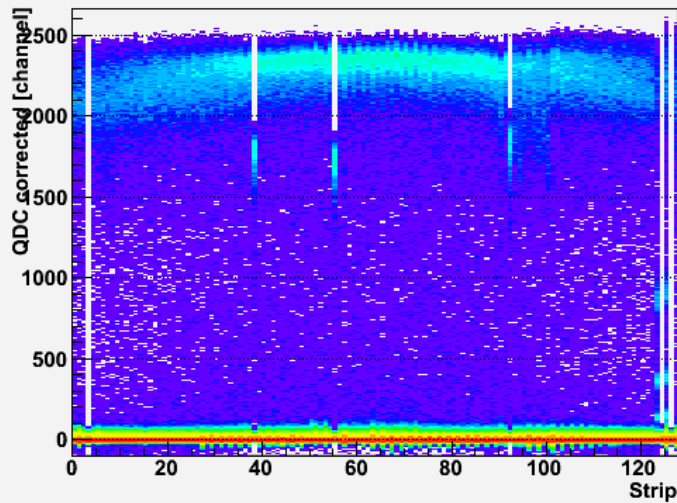
Side L1_L_Pos Profile (ADC=SpADC_1)



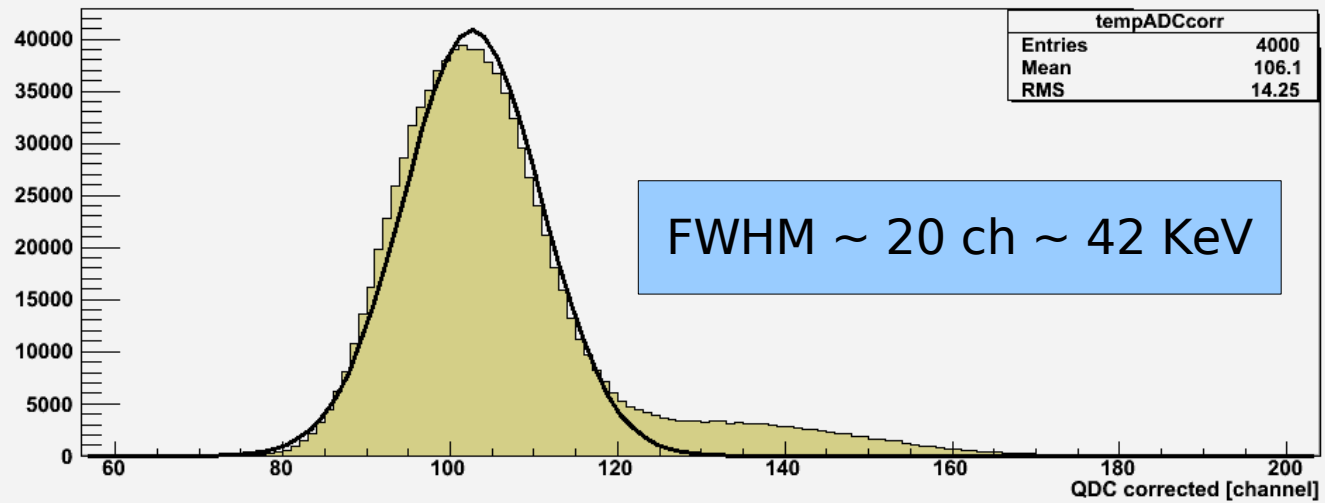
Segment QDC L1_L_Pos 050 (ADC=SpADC_1 input=0 channel=050)



Side L1_L_Pos Corrected Profile (ADC=SpADC_1)

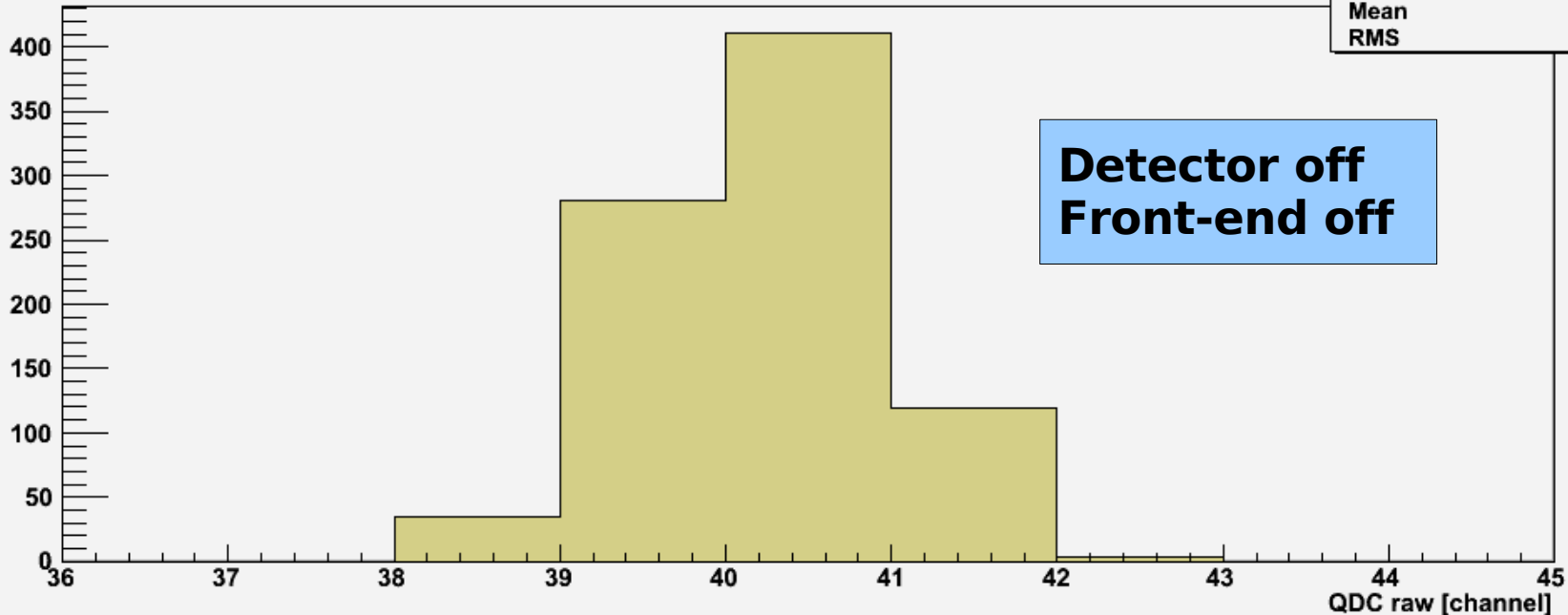


segment corrected L1_L_Pos 050 (ADC=SpADC_1 input=0 channel=050)



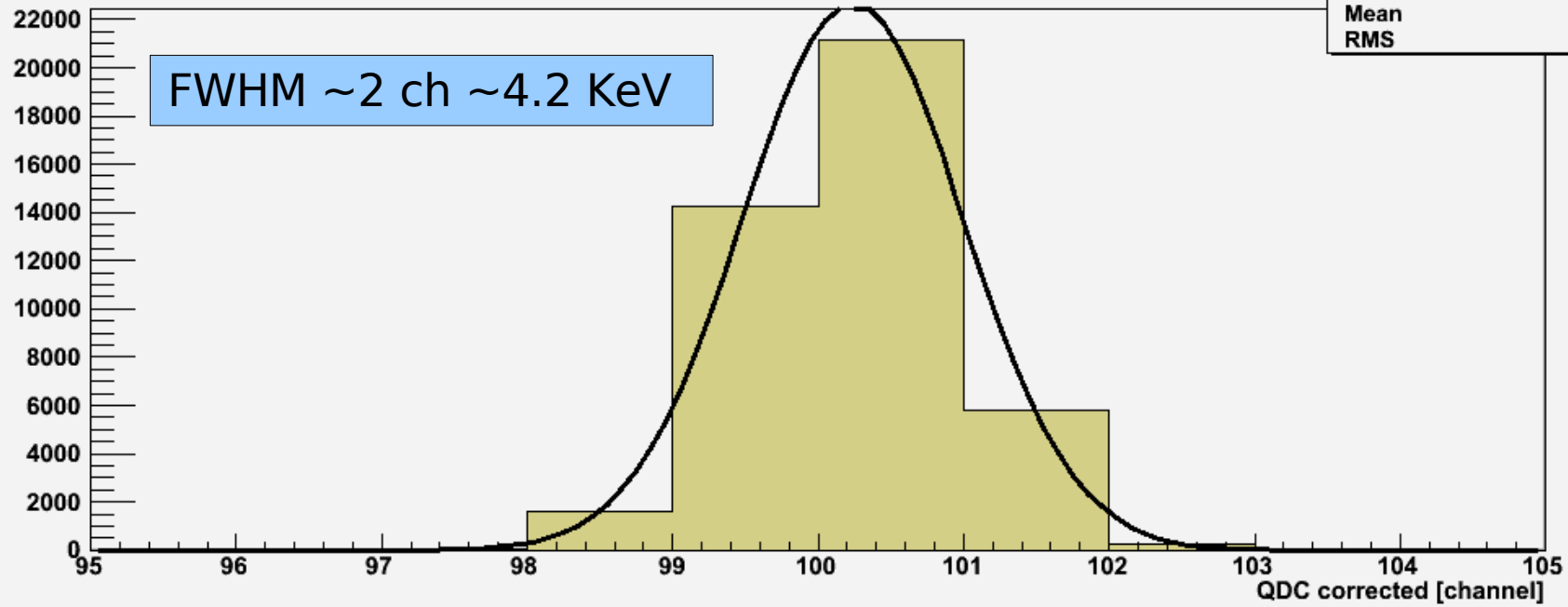
Segment QDC L1_L_Pos 050 (ADC=SpADC_1 input=0 channel=050)

| tempADC | |
|---------|--------|
| Entries | 4000 |
| Mean | 40.24 |
| RMS | 0.7647 |



segment corrected L1_L_Pos 050 (ADC=SpADC_1 input=0 channel=050)

| tempADCcorr | |
|-------------|--------|
| Entries | 4000 |
| Mean | 100.2 |
| RMS | 0.7583 |



- ADC resolution: 1 ch = ~ 2.1 KeV
- Pedestal width is ~ 42 KeV (VME system ~ 60 KeV)

- Readout is working at 10 MHz
- Software needs development/tuning performance

Conclusion: vertex boards will be used in November

Goal:
One **Complete readout system**
for November beam-time
(Depolarization studies)

- ♦ 6 (upgraded) Vertex boards (1 for detector)
[2 complete telescopes (3 layer each)]
- ♦ 1 LVDS crate (1 LVDS TDC)
- ♦ 1 VME crate
- ♦ 1 VME trigger unit (A.Cotta) / VME scalers
- ♦ Implementation in ANKE
- ♦ Software (S.Trusov talk)

Software:

- Sequencer programming (S. Chiozzi/see later)
- Changes in server software to go to high speed readout (P. Wüstner)
- Client program (GUI) to control (M.Nekipelov)
- Rest of software (S. Trusov)
- Xilinx modifications: common-mode & zero suppression (ZEL)

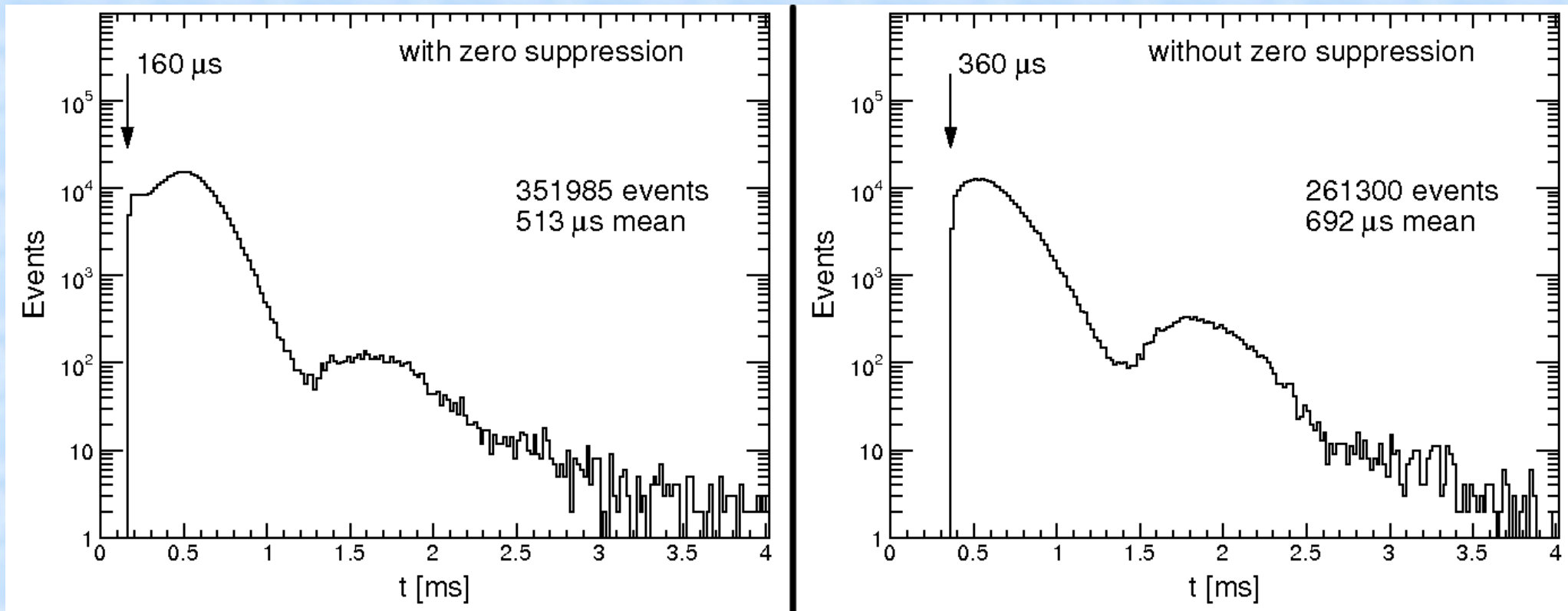
VME system deadtime

Old system (VME ADCs VME Sequencer, 2 detectors, 5MHz, [1])

Minimum Deadtime (without zero suppression): 360 μs

Minimum Deadtime (with zero suppression): 160 μs

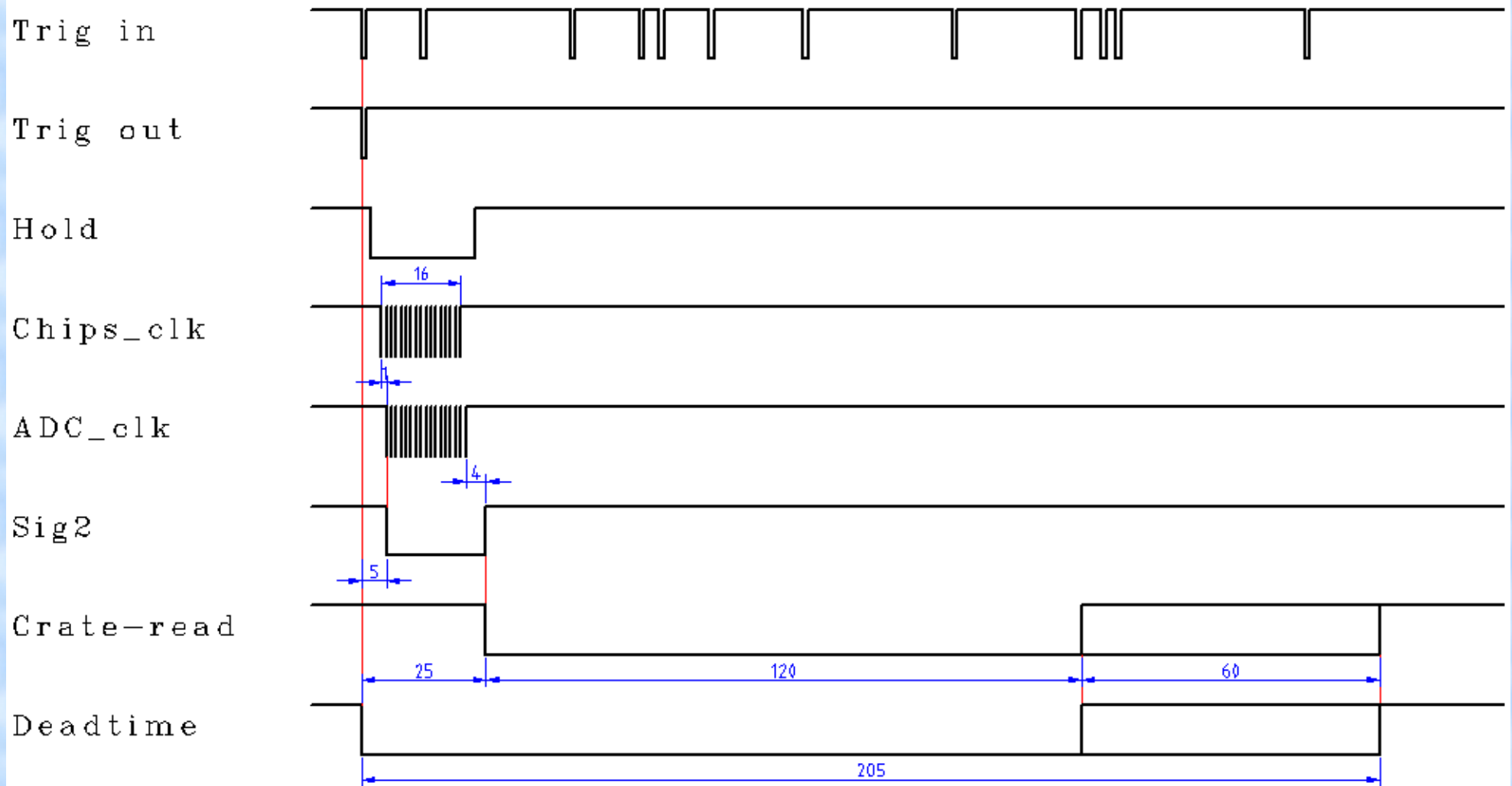
ADC ready in $\sim 50 \mu\text{s}$ ($\rightarrow \sim 25 \mu\text{s}$)



[1] Identification and Tracking of low energy spectator protons
A.Mussgiller, 2005

Data from test LVDS system (10 MHz):

Event size: 1336 byte/ev (1.3GB/10⁶ev)
Countrate(det surface): ~1000 Hz
Acquired event rate: ~600 Hz



All times in μs

Conclusion

**Good readout system,
still needs software development**